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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,715	OLZAK ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Response filed November 03, 2003 (Certificate of Mailing date: October 31, 2003). Claims 1-32 remain pending in the instant Application.

Claim Objections

2. Claims 15, 17 and 18 are objected to because of the following informalities:

In Claim 15, line 2: after "interconnected" change "layer" to --layers--.

In Claim 17, line 1: after "coupling" insert --means--.

In Claim 18, line 2: after "coupling" insert --means--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 20-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20, lines 1-2, recite "[a] method for adapting a first surface mounted device having a first quantity of input/output leads **to a replace a** second surface mounted device...", wherein the phrase in bold emphasis renders the preamble meaningless.

The Examiner will interpret the claim language by **omitting "a"** after "to" in line 2 of the claim. Clarification of the claim language is required.

Claim 20, line 9 recites "after assembly to a **using** printed circuit board," wherein the word in bold emphasis renders the phrase indefinite. What is a "**using** printed circuit board?" Is it different than "a printed circuit board" in lines 6-7 of the claim, or "printed circuit board" in line 2 of Claim 24? The Examiner will interpret "a **using** printed circuit board" by omitting "using" and reading *a printed circuit board* instead, in the art rejection of Claim 20, below. Clarification of the claim language is required.

As to Claim 21, line 3: for the same reason as indicated above for Claim 20, the Examiner will omit the word "using" and read *a printed circuit board* instead. Clarification of the claim language is required.

Claims 22-24 depend from defective base Claim 20 and therefore inherit the defects of the base claim.

As to Claim 25, line 2: for the same reason as indicated above for Claims 20 and 21, the Examiner will omit the word "using" and read *a printed circuit board* instead. Clarification of the claim language is required.

As to Claim 26, line 6: for the same reason as indicated above for Claims 20, 21 and 25, the Examiner will omit the word "using" and read *the printed circuit board* instead. Clarification of the claim language is required.

As to Claim 27, lines 3-9 recite "a printed circuit board" and "the printed circuit board, while lines 10-11 recite "the printed circuit board," but the "printed circuit board" recitation of lines 10-11 is not the same as the "printed circuit board" of lines 3-9. Based

on the Applicant's disclosure, the "printed circuit board" of lines 3-9 corresponds to the adapter board and the printed circuit board of lines 10-11 corresponds to the parent printed circuit board. The claim language, however, does NOT make this distinction clear. Accordingly, the above interpretation will be the one used by the Examiner for the art rejections of Claims 27-31, below. Clarification of claim language is required.

Claim 28 depends from defective base Claim 27 and therefore inherits the defects of the base claim.

As to Claim 29, lines 1-3 recite "a solder joint whereby the signal carriers are electrically and mechanically joined to corresponding contact areas of **the printed circuit board**" (bold emphasis added). However, as indicated in base Claim 27, it is not made clear which board is intended. The Examiner will interpret "the printed circuit board" to be *the parent printed circuit board* supported by the Applicant's disclosure. Clarification of claim language is required.

Claims 30-32 depend from defective base Claim 27 and therefore inherit the defects of the base claim.

Rejections Based On Prior Art

5. The following references were relied upon for the rejections hereinbelow:

Tsai et al. (US 6,395,996 B1)

Chu et al. (US 5,941,447)

Yamaguchi et al. (US 6,147,876)

Dalal et al. (US 5,796,591)

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-4, 6-14 and 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al.

As to Claim 1, Yamaguchi et al. discloses: an insulating body 100D (Fig. 24) having offset first (top) and second (bottom) surfaces (Figs. 12 and 13, respectively); a pattern 101D of surface mount (flip-chip) solder pads 131 (analogous to the wire-bond solder pads 107 mentioned and shown in embodiments other than the flip-chip embodiment of Figs. 24-26, the latter embodiment being the one to which the Examiner is primarily referring in the present rejection) formed on the first surface (Fig. 24; col.11: 20-26; col.13: 45-47; col.14: 2-5 and 19-22); a pattern of signal carriers 105

communicating between the first and second surfaces (Fig. 24), each of the signal carriers 105 (specifically, metallization 105a, as shown in Fig. 7) being at least partially exposed in an area **between** the first and second surfaces (Figs. 24 and 25; col.9: 50-58; col.13: 41-45) and adjacent to the second surface (Fig. 13 shows the second surface and signal carriers 105a adjacent thereto); and a plurality of signal lines 109 electrically coupling one or more of surface mount solder pads 131 with predetermined ones of signal carriers 105a (Figs. 24 and 25; col.13: 48-50).

As to Claim 2, Yamaguchi et al. further discloses a pattern of electrical contacts--i.e., the surface metallization adjacent the edge of body 100D (Figs. 13, 24 and 25)--formed **on** the second surface and being electrically coupled to different ones of signal carriers 105 (i.e., said surface metallization adjacent the edge of body 100D is coupled to both portions 105a and 105b of signal carriers 105, as shown in Figs. 7, 13, 24 and 25).

As to Claim 3, Yamaguchi et al. further discloses, in Figs. 10 and 21, insulating body 100D comprises a signal layer 116 laminated between the first and second surfaces with one or more of the plurality of signal lines 119 (the extension of surface signal lines 109 connected thereto by vias 112) being formed on the signal layer 116 (col.9: 61-col.10: 4; col.13: 54-59).

As to Claim 4, Yamaguchi et al. further discloses each of the signal carriers 105 comprises an electrically conductive material 105a formed on an interior passage that communicates between the first and second surfaces (Figs. 7, 24 and 25; col.9: 53-58).

As to Claim 6, Yamaguchi et al. discloses: a printed circuit board (PCB) 100D (Fig. 24) having a top layer (Fig. 12) and a bottom layer (Fig. 13), and a first footprint 101D formed on the top layer of PCB 100D for receiving a first surface mount device 201D (Fig. 24; col.14: 19-22), and a second footprint on the bottom layer of PCB 100D (i.e., the second footprint comprising the electrical contacts of the bottom layer that are adjacent the edge of PCB 100D and coupled to both portions 105a and 105b of input/output lines 105, as shown in Fig. 13) for simulating a second surface mount device (i.e., for mounting the bottom layer, shown in Fig. 13, of PCB 100D onto the surface of motherboard 1, as shown in Fig. 26); a plurality of input/output (I/O) lines 105 connected between the first footprint 131 and one or more of a plurality of contacts corresponding to the second footprint (as discussed, above), at least a portion of the I/O 105 adjacent to the bottom layer being exposed between the top and bottom layers (Figs. 13, 24 and 25).

As to Claim 7, Yamaguchi et al. further discloses a plurality of solder pads 131 (analogous to the wire-bond solder pads 107 mentioned and shown in embodiments other than the flip-chip embodiment of Figs. 24-26, the latter embodiment being the one to which the Examiner is primarily referring) formed on the top layer and corresponding to the first foot print 101D (Fig. 24; col.1: 20-26; col.13: 45-47; col.14: 2-5 and 19-22).

As to Claim 8, Yamaguchi et al. further discloses I/O lines 105 couple one or more of solder pads 131 on the top layer to one or more of the plurality of electrical contacts on the bottom layer (Figs. 13 and 24; col.9: 50-58; col.13: 48-50).

As to Claim 9, Yamaguchi et al. further discloses the electrical contacts further comprise a plurality of solder pads formed on the bottom layer (Fig. 13) and corresponding to the second footprint (Figs. 13, 25 and 26; col.11: 20-26; col.13: 41-45).

As to Claim 10, Yamaguchi et al. further discloses each of the plurality of I/O lines 105 further comprises a quantity of electrically conductive metal 105a deposited in a groove that communicates between the top and bottom layers (Figs. 7, 24 and 25; col.9: 53-58).

As to Claim 11, Yamaguchi et al. further discloses the second footprint is different from the first footprint (compare the second footprint defined by the electrical contacts on the bottom surface, shown in Fig. 13, with the first footprint 101D shown in Fig. 24).

As to Claim 12, Yamaguchi et al. discloses: a printed circuit board (PCB) 100D having a top layer (Fig. 12) and a bottom layer (Fig. 13); a pattern 101D of solder pads 131 formed on the top layer of PCB 100D, the pattern 101D being structured for receiving a first surface mount device 201D (Figs. 24 and 25); a plurality of vias along a periphery of PCB 100D (Figs. 24 and 25) and communicating between the top layer and the bottom layer (Figs. 12 and 13), each of the vias having a quantity of electrically conductive material 105a deposited therein (Figs. 7, 24 and 25; col.9: 50-58; col.13: 41-45); an electrical signal line 109 coupled between one of solder pads 131 and one of the vias (Figs. 24 and 25; col.13: 48-50); and a pattern of electrical contacts formed on the bottom layer of PCB 100D (Fig. 13) being structured to simulate a second surface

mount device (i.e., for mounting the bottom layer, shown in Fig. 13, of PCB 100D onto the surface of motherboard 1, as shown in Fig. 26).

As to Claim 13, Yamaguchi et al. further discloses at least a portion of the electrically conductive material 105a in each of the plurality of vias adjacent to the corresponding electrical contacts formed on the bottom layer is exposed between the top and bottom layers (Figs. 13, 24 and 25).

As to Claim 14, Yamaguchi et al. further discloses each of the plurality of vias further comprises an electrically conductive material 105a plated on an interior surface of a partial cylindrical passage (Figs. 24 and 25; col.9: 53-58).

As to Claim 16, Yamaguchi et al. discloses: a body means 100D for supporting a first surface mounted device 201D relative to a printed circuit board 1 (Figs. 24, 25 and 26); a first interconnecting means 131 being positioned on a first surface of body means 100D for electrically interconnecting to a first surface mounted device 201D (col.14: 19-22); a second interconnecting means being positioned on a second surface of body means 100D--i.e., the pattern of electrical contacts formed on the second (bottom) surface of body means 100D, as shown in Fig. 13--for electrically interconnecting to a printed circuit board 1 structured to receive a second surface mounted device 5D (Fig. 26); and means 105 for electrically coupling the first and second electrically interconnecting means, at least a portion 105a of the electrically coupling means 105 being exposed between the first and second surfaces of body means 100D (Figs. 12, 13, 24 and 25; col.9: 50-58; col.13: 48-50).

As to Claim 17, Yamaguchi et al. further discloses that electrically coupling means 105 further comprises signal communication means spanning between the first and second surfaces along a peripheral surface of body means 100D (Figs. 24 and 25; col.9: 50-58).

As to Claim 18, Yamaguchi et al. further discloses the exposed portion 105a of the electrically coupling means 105 is positioned adjacent to the second (bottom) surface of body means 100D (Figs. 7 and 13; col.9: 50-58).

As to Claim 19, Yamaguchi et al. further discloses first interconnecting means 131 further comprises means for forming an electrically conductive solder joint (Fig. 24; col.11: 20-26; col.13: 45-47; col.14: 2-5 and 19-22).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 5 and 20-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Dalal et al.

As to Claim 5:

I. Yamaguchi et al. discloses all the limitations of the claim including signal lines 109 coupling a function of surface mount device 201D to signal carriers 105 (Fig. 25) but does not teach that signal lines 109 couple a function of a replacement surface

mount device 201D to a signal carrier 105 that corresponds to a position in the pattern of signal carriers 105 that is associated with a similar function provided by a replaced surface mount device 201D; in other words, Yamaguchi et al. does not teach that device 201D is a replacement device that has replaced a functionally similar device 201D on the surface mount solder pads 131 that are connected to said signal lines 109 that couple the function of device 201D to signal carriers 105.

II. Dalal et al. discloses replacement of surface mounted devices enabled by a surface mount device 30 having flip-chip electrode leads formed as high melting point (HMP) solder bumps 38 having low (eutectic) melting point (LMP) caps 41 that establish good electromechanical connection with the circuit board (Fig. 5; col.8: 44-57) and easy subsequent removal of the joined surface mount device for the purpose of "replacement without mechanically or thermally affecting other components on the board (col.6: 28-34).

III. Since Yamaguchi et al. teaches that the I/O leads of the first surface mounted device are flip-chip electrode leads (col.14: 19-22), and also teaches testing the surface mount multichip module 5D (by testing for defective devices 201D using second electrical interconnecting means 105) before surface mounting the module 5D to printed circuit board 1 (col.14: 26-30) and furthermore, since both Yamaguchi et al. and Dalal et al. are both in the art of solder mounting electronic components to a circuit board to form reliable electronic packages, then the concept of replacing a defective surface mount device with another of the same type of surface mount device by solder reflow and enabling such a solder-reworked replacement by fabricating the flip-chip bump

leads to comprise HMP solder capped with eutectic (LMP) solder, as taught by Dalal et al., would have been readily recognized as useful for the reliable fabrication of, and post-testing flip-chip device replacement on, the multichip modules 5D of Yamaguchi et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the flip-chip leads of surface mount devices 201D of Yamaguchi et al. with the flip-chip bump lead HMT/LMT structure taught by Dalal et al. in order to easily and safely replace a defective second surface mounted device 201D in Yamaguchi et al. with a known good surface mount device 201D, said defective device 201D being easily and safely removed from the module board 100D of multichip module 5D due to the flip-chip HMT/LMT bump lead structure of the surface mount devices taught by Dalal et al., and the replacement surface mount device placed on the same surface mount solder pads 131 such that the signal lines 109 couple a function of the replacement surface mount device 201D to a signal carrier 105 that corresponds to a position in the pattern of signal carriers 105 that is associated with a similar function provided by the replaced surface mount device 201D, thus enabling the multichip module 5D to perform its intended operations on system printed circuit board 1.

As to Claim 20:

I. Yamaguchi et al. discloses a method comprising: providing first electrical interconnecting means 131 (on a multichip module 5D) structured for coupling to I/O leads (i.e., flip-chip electrode leads) of first surface mounted device 201D (Figs. 24 and

25; col.14: 19-22); providing second electrical interconnecting means 105 structured for coupling to a printed circuit board 1 that is structured to receive a second surface mounted device (i.e., another multichip module 5D adjacent to the above-mentioned multichip module 5D; Figs. 25 and 26), including providing the second electrical interconnecting means 105 at a portion of an adapter body 100D (i.e., the periphery of the adapter body 100D) that remains available for visual inspection after assembly to a printed circuit board 1 (col.9: 50-58; col.13: 41-45); and providing signal conduction means 109 for carrying input/output (I/O) signals between the first and second electrical interconnecting means 131 and 105, respectively (col.13: 48-50).

II. Yamaguchi et al. does not teach the method includes adapting the first surface mounted device 201D **to replace a second surface mounted device 201D having a second quantity of I/O leads**.

III. Dalal et al. discloses replacement of surface mounted devices enabled by a surface mount device 30 having flip-chip electrode leads formed as high melting point (HMP) solder bumps 38 having low (eutectic) melting point (LMP) caps 41 that establish good electromechanical connection with the circuit board (Fig. 5; col.8: 44-57) and easy subsequent removal of the joined surface mount device for the purpose of "replacement without mechanically or thermally affecting other components on the board (col.6: 28-34).

IV. Since Yamaguchi et al. teaches that the I/O leads of the first surface mounted device are flip-chip electrode leads (col.14: 19-22), and also teaches testing the surface mount multichip module 5D (by testing for defective devices 201D using

second electrical interconnecting means 105) before surface mounting the module 5D to printed circuit board 1 (col.14: 26-30) and furthermore, since both Yamaguchi et al. and Dalal et al. are both in the art of solder mounting electronic components to a circuit board to form reliable electronic packages, then the concept of replacing a defective surface mount device with another of the same type of surface mount device by solder reflow and enabling such a solder-reworked replacement by fabricating the flip-chip bump leads to comprise HMP solder capped with eutectic (LMP) solder, as taught by Dalal et al., would have been readily recognized as useful for the reliable fabrication of, and post-testing flip-chip device replacement on, the multichip modules 5D of Yamaguchi et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the flip-chip leads of surface mount devices 201D of Yamaguchi et al. with the flip-chip bump lead HMT/LMT structure taught by Dalal et al. in order to adapt a first surface mounted device 201D to easily and safely replace a defective second surface mounted device 201D in Yamaguchi et al., said defective device 201D being easily and safely removed from the module board 100D of multichip module 5D due to the flip-chip HMT/LMT bump lead structure of the surface mount devices taught by Dalal et al.

As to Claim 21, modified Yamaguchi et al. further discloses providing at least a portion 105a of the second electrical interconnecting means 105 along an exterior surface of adapter body 100D (Figs. 7 and 24).

As to Claim 22, modified Yamaguchi et al. further discloses forming a first quantity of solder pads 131 on a top layer of adapter body 100D in a pattern structured to receive the I/O leads (i.e., flip-chip electrodes) of first surface mounted device 201D (Fig. 24; col.11: 20-26; col.13: 45-47; col.14: 2-5 and 19-22).

As to Claim 23, modified Yamaguchi et al. further discloses soldering the I/O leads of first surface mounted device 201D to corresponding ones of the solder pads 131 (Fig. 25; col.11: 20-26; col.13: 45-47; col.14: 2-5 and 19-22).

As to Claim 24, modified Yamaguchi et al. further discloses forming a quantity of contacts on a bottom layer of adapter 100D (Fig. 13) in a pattern structured in a pattern simulating I/O leads of the second surface mounted device 201D (Figs. 13, 24, 25 and 26).

As to Claim 25, modified Yamaguchi et al. further discloses soldering the contacts on the bottom layer of adapter body 100D on a printed circuit board 1 corresponding (by way of second electrical interconnecting means 105, signal conduction means 109 and solder pads 131) to I/O leads (i.e., the flip-chip electrodes) of the second surface mounted device 201D (Fig. 26; col.9: 50-53; col.11: 20-26; col.13: 41-53; col.14: 32-35).

As to Claim 26, modified Yamaguchi et al. further discloses providing signal conduction means 109 between one of the first electrical interconnecting means 131 structured to couple to one I/O lead of the first surface mount device 201D for providing a first I/O signal and one of the second electrical interconnecting means 105 structured couple to a contact on printed circuit board 1 that is structured to communicate with an

I/O signal of the (replaced) second surface mounted device 201D similar to the first I/O signal of the first surface mount device 201D (Figs. 24-26; col.13: 34-57; col.14: 32-35).

As to Claim 27:

I. Yamaguchi et al. discloses a parent printed circuit board assembly, the assembly comprising: a printed circuit board (PCB) 100D (Fig. 24) having a top layer (Fig. 12) and a bottom layer (Fig. 13); a footprint 101D formed on the top layer of first PCB 100D (Fig. 24; col.13: 34-40 and 45-47); a first surface mount device 201D (having flip-chip electrode leads; col.14: 19-22) being mounted to footprint 101D on the top layer of PCB 100D (Figs. 24 and 25; col.13: 34-40); a plurality of signal carriers 105 positioned along different peripheral edges of PCB 100D and extended between the top and bottom layers of PCB 100D and being at least partially exposed in an area adjacent to the bottom layer (Figs. 13, 24 and 25; col.9: 50-58; col.13: 41-45), each of the signal carriers 105 being electrically and mechanically joined to a corresponding contact area of a parent PCB 1 (Fig. 26; col.13: 41-45); and a plurality of signal lines 109 communicating between corresponding contact areas 131 of footprint 101D and at least a portion of the signal carriers 105 (Figs. 24 and 25; col.13: 48-50).

II. Yamaguchi et al. does not teach that the parent printed circuit board assembly has a replacement surface mount device 201D substituted for an original surface mount device 201D.

III. Dalal et al. discloses replacement of surface mounted devices enabled by a surface mount device 30 having flip-chip electrode leads formed as high melting point (HMP) solder bumps 38 having low (eutectic) melting point (LMP) caps 41 that establish

good electromechanical connection with the circuit board (Fig. 5; col.8: 44-57) and easy subsequent removal of the joined surface mount device for the purpose of "replacement without mechanically or thermally affecting other components on the board (col.6: 28-34).

IV. Since Yamaguchi et al. teaches that the I/O leads of the first surface mounted device are flip-chip electrode leads (col.14: 19-22), and also teaches testing the surface mount multichip module 5D (by testing for defective devices 201D using second electrical interconnecting means 105) before surface mounting the module 5D to printed circuit board 1 (col.14: 26-30) and furthermore, since both Yamaguchi et al. and Dalal et al. are both in the art of solder mounting electronic components to a circuit board to form reliable electronic packages, then the concept of replacing a defective surface mount device with another of the same type of surface mount device by solder reflow and enabling such a solder-reworked replacement by fabricating the flip-chip bump leads to comprise HMP solder capped with eutectic (LMP) solder, as taught by Dalal et al., would have been readily recognized as useful for the reliable fabrication of, and post-testing flip-chip device replacement on, the multichip modules 5D of Yamaguchi et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the flip-chip leads of surface mount devices 201D of Yamaguchi et al. with the flip-chip bump lead HMT/LMT structure taught by Dalal et al. in order to easily and safely replace the defective second surface mounted device 201D in Yamaguchi et al. with the known good first surface mount device 201D,

said defective second device 201D being easily and safely removed from the module board 100D of multichip module 5D due to the flip-chip HMT/LMT bump lead structure of the surface mount devices taught by Dalal et al., thus enabling the multichip module 5D to perform its intended operations on parent printed circuit board 1.

As to Claim 28, modified Yamaguchi et al. further discloses an electrical contact pad formed on the bottom layers of PCB 100D at each of the signal carriers 105 (Fig. 13).

As to Claim 29, modified Yamaguchi et al. further discloses a solder joint whereby signal carriers 105 are electrically and mechanically joined to corresponding contact areas of parent PCB 1, each of the solder joints inherently being at least partially formed on the partially exposed portion of each of the signal carriers 105 due to inherent solder wicking along at least a portion of the solder-wettable conductive material 105a of signal carriers 105 (Fig. 26; col.9: 50-58; col.13: 41-45).

As to Claim 30, modified Yamaguchi et al. further discloses the replacement surface mount device 201D is a replacement device 201D having the same I/O lead arrangement, as taught by Dalal et al. (see Dalal et al., col.6: 28-34), structured to provide input/output (I/O) signals substantially identical to I/O signals provided by a replaced device 201D (Figs. 25 and 26; col.13: 34-57) but does not disclose that the replacement device 201D is of the same functional type as the replaced device 201D. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace a defective surface mount device 201D having a particular function and I/O lead arrangement with another surface mount device 201D

having the same function as well as the same I/O lead arrangement of the replaced device on the multichip module 5D of modified Yamaguchi et al. in order to provide the required functionality of the replaced device 201D that enables multichip module 5D to perform the operations, for which it was originally designed, on parent PCB 1.

As to Claim 31, Yamaguchi et al. further discloses the I/O signals of replacement device 201D are coupled to contact areas 131 of the PCB 100D structured to interface with corresponding I/O signals of the replaced device 201D (col.13: 34-40; col.14: 19-22).

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Chu et al. and Tsai et al.

I. Yamaguchi et al. discloses PCB 100D comprises a plurality of interconnected layers including a signal layer (i.e., the conductor layers of inner layer 116 connected to signal lines 109; Fig. 10 and col.9: 66-col.10: 2).

II. Yamaguchi et al. does not explicitly teach a ground layer among the interconnected layers of PCB 100D. However, Yamaguchi et al. does teach that PCB 100D has a capacitor 122 built into the inner layers of PCB 100D and comprising conductive "plate" layers 119 and dielectric layer 126 (Fig. 23; col.12: 66-67; col.13: 5-14).

III. Chu et al. discloses, in Fig. 6, that it is old and well-known to use built-in capacitors 70 as decoupling capacitors to decouple switching noise in surface mount devices 20, 40 (col.8: 54-61; col.9: 4-10) and Tsai et al. discloses, in Figs. 2 and 4, that it is old and well-known to use built-in capacitors to suppress noise due to voltage

fluctuations between the power and ground layers of a multilayer board operating at high frequencies (col.1: 15-26; col.2: 30-47; col.3: 13-18).

IV. Since Yamaguchi et al., Chu et al. and Tsai et al. all disclose a capacitor built-into a PCB carrying IC surface mount devices communicating and switching signals at high frequencies, then using the built-in capacitor 122 of Yamaguchi et al. as a decoupling capacitor for suppressing noise and ensuring the reliable functioning of the PCB and the surface mount devices thereon, as taught by Chu et al. and Tsai et al., would have been readily recognized as beneficial to the reliability of adapter comprising the PCB 100D and the surface mount devices thereon of Yamaguchi et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conductive layers 119 of Yamaguchi et al. such that one of the conductive layers 119 is a ground layer and the other a power layer such that capacitor 122 functions as a decoupling capacitor that decouples the switching noise from the surface mount device 201D and suppresses noise generated by high frequency voltage fluctuations between the power and ground layers 119 of the PCB 100D, as taught by Chu et al. and Tsai et al., in order to ensure reliable operation of the adapter of Yamaguchi et al.

Allowable Subject Matter

11. Claim 32 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 32, patentability resides in the limitation wherein *fewer of the corresponding contact areas of the footprint are provided for the replacement device than the contact areas provided on the printed circuit board for the replaced device*, in combination with the other limitations of the claim.

13. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Examiner's Remarks

14. The Examiner acknowledges Applicant's affidavit under 37 CFR § 1.131 filed concurrently with the instant Response cited above in section 1. Said affidavit has been reviewed and accepted, and, consequently, the Okada et al. reference (US 6,534,726 B1), relied upon for the rejections of Claims 1, 2 and 4-31 in the previous Office Action of July 03, 2003, is hereby disqualified and the rejections withdrawn.

15. The arguments in the Applicant's instant Response regarding patentability of Claims 1, 2 and 4-31 of the instant Application over Okada et al. have been considered but are moot in view of the new ground(s) of rejection. Due to the new grounds of rejection raised by the Examiner, the present Office Action is made NON-FINAL.

16. The indicated allowability of Claim 3, in the previous Office Action of July 03, 2003, is withdrawn in view of the newly discovered reference to Yamaguchi et al. and the rejection based on the newly cited reference has been set forth, above.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references disclose chip modules including metallized "half" through-holes (castellations) at the periphery of the circuit boards that electrically communicate between the top surface of the board and the bottom surface of the board and are used to electromechanically connect the module to a system printed circuit board:

Downie et al. (US 5,471,368) : Figs. 4 and 5.

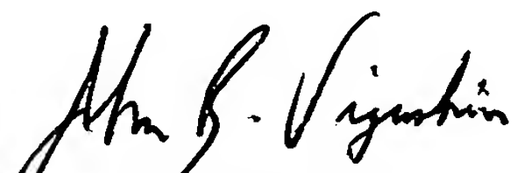
Thompson et al. (US 5,293,067) : Figs. 1 and 2.

Prokop (US 4,437,141): Figs. 5 and 6.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205 (Crystal City campus) or 571-272-1936 (Carlyle campus). The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



John B. Vigushin
Primary Examiner
Art Unit 2827

jbv
January 21, 2004